

## APPLICATION DATA SHEET

### APPLICATION INFORMATION

Filing Date:: 10-10-2003  
Application Type:: Regular  
Subject Matter:: Utility  
Title:: Structures and Methods of Testing  
Interconnect Structures in  
Programmable Logic Devices  
Attorney Docket Number:: X-1412 US  
Request for Early Pub?:: No  
Request for Non-Pub?:: Yes  
Total Drawing Sheets:: 07  
Small Entity?:: No  
Petition included?:: No

### APPLICANT INFORMATION

Applicant Authority Type:: Inventor  
Primary Citizenship Ctry:: US  
Status:: Full Capacity  
Given Name:: Trevor  
Middle Name:: J.  
Family Name:: Bauer  
Street:: 3860 Campo Court  
City:: Boulder  
State or Province:: Colorado  
Postal or Zip Code:: 80301

Applicant Authority Type:: Inventor  
Primary Citizenship Ctry:: US  
Status:: Full Capacity  
Given Name:: Steven  
Middle Name:: P.  
Family Name:: Young  
Street:: 1180 Pintail Circle

City:: Boulder  
State or Province:: Colorado  
Postal or Zip Code:: 80303  
  
Applicant Authority Type:: Inventor  
Primary Citizenship Ctry:: US  
Status:: Full Capacity  
Given Name:: Ramakrishna  
Middle Name:: K.  
Family Name:: Tanikella  
Street:: 2898 Aurora Avenue  
City:: Boulder  
State or Province:: Colorado  
Postal or Zip Code:: 80303

#### **CORRESPONDENCE INFORMATION**

Correspondence Customer Number:: 24309

#### **REPRESENTATIVE INFORMATION**

<b>Representative Customer Number::</b>	<b>24309</b>	
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#### **ASSIGNEE INFORMATION**

Assignee Name:: Xilinx, Inc.  
Street:: 2100 Logic Drive  
City:: San Jose  
State or Province:: California  
Postal or Zip Code:: 95124